REMARKS

Claims 28-51 remain in the present application. Applicants respectfully request further examination and reconsideration of the rejections.

Claim Rejections – 35 U.S.C. §102

Claims 28-33, 35, 37-42 and 44

Claims 28-33, 35, 37-42 and 44 are rejected in the present Office Action under 35 U.S.C. §102(b) as being anticipated by United States Patent Number 3,805,247 to Zucker et al. (referred to herein as "Zucker"). Applicants have reviewed the cited reference and respectfully submit that the embodiments of the present invention as recited in Claims 28-33, 35, 37-42 and 44 are neither anticipated nor rendered obvious by Zucker for the following reasons.

Applicant respectfully directs the Examiner to independent Claim 28, which recites a system comprising (emphasis added):

> a plurality of memory resources;
> a plurality of peripheral resources;
> a plurality of processors;
> a memory controller coupled to said plurality of processors and said plurality of memory resources, wherein said memory controller comprises a first resource controller for controlling access of said plurality of processors to said plurality of memory resources, and wherein said first resource controller is further operable to implement respective buses for coupling said plurality of processors to said plurality of memory resources; and
> a peripheral controller coupled to said plurality of processors and said plurality of peripheral resources, wherein said peripheral controller comprises a second resource controller for controlling access of said plurality of processors to said plurality of peripheral resources, and wherein said first resource controller is further operable to implement respective buses for coupling said plurality of processors to said plurality of peripheral resources.

Independent Claim 37 recites limitations similar to independent Claim 28. Claims 29-33, 35, 38-42 and 44 depend from their respective independent Claims and recite further limitations to the claimed invention.

Applicants respectfully submit that Zucker fails to teach or suggest the limitations of "wherein said first resource controller is further operable to implement respective buses for coupling said plurality of processors to said plurality of memory resources" as recited in independent Claim 28. As recited and described in the present application, a first resource controller is operable to implement respective buses for coupling a plurality of processors to a plurality of memory resources. In this manner, a first processor may access a first memory resource independently of a second processor accessing a second memory resource.

In contrast to the claimed embodiments, Applicants fail to find any teaching or suggestion in Zucker of respective buses for coupling a plurality of processors to a plurality of memory resources as claimed. Instead, Applicants understand Zucker to teach resolving conflicts between a plurality of processors attempting to access *the same memory module* using a "lock instruction" (col. 12, lines 23-32). Further, assuming arguendo that memory controller 80 as taught by Zucker is analogous to a resource controller of a memory controller as claimed, although Zucker may teach that memory controller 80 is for resolving conflicts between processors (col. 10, lines 41-48), Applicants respectfully submit that Zucker fails to teach that memory controller 80 is operable to implement

respective buses for coupling a plurality of processors to a plurality of memory resources as claimed. Accordingly, Applicants reiterate that Zucker fails to teach or suggest the limitations of "wherein said first resource controller is further operable to implement respective buses for coupling said plurality of processors to said plurality of memory resources" as recited in independent Claim 28.

Applicants respectfully submit that Zucker fails to teach or suggest the limitations of "wherein said first resource controller is further operable to implement respective buses for coupling said plurality of processors to said plurality of peripheral resources" as recited in independent Claim 28. As recited and described in the present application, a second resource controller is operable to implement respective buses for coupling a plurality of processors to a plurality of peripheral resources. In this manner, a first processor may access a first peripheral resource independently of a second processor accessing a second peripheral resource.

In contrast to the claimed embodiments, Applicants fail to find any teaching or suggestion in Zucker of respective buses for coupling a plurality of processors to a plurality of peripheral resources as claimed. Instead, Applicants understand Zucker to teach resolving conflicts between a plurality of processors attempting to access *the same device* using a "lock instruction" (col. 12, lines 23-32). Further, assuming arguendo that device controller 82 as taught by Zucker is analogous to a resource controller of a peripheral controller as claimed, although Zucker may teach that device controller 82 is for resolving conflicts between

processors (col. 10, lines 49-53), Applicants respectfully submit that Zucker fails to teach that device controller 82 is operable to implement respective buses for coupling a plurality of processors to a plurality of peripheral resources as claimed. Accordingly, Applicants reiterate that Zucker fails to teach or suggest the limitations of "wherein said second resource controller is further operable to implement respective buses for coupling said plurality of processors to said plurality of peripheral resources" as recited in independent Claim 28.

Applicants respectfully submit that Zucker fails to teach or suggest the limitations of "wherein said first resource controller is further operable to enable each of said plurality of processors to simultaneously access a different memory resource of said plurality of memory resources" as recited in Claim 30, and similarly recited in Claim 39. As recited and described in the present application, the first resource controller is operable to enable each of the plurality of processors to simultaneously access a different memory resource of the plurality of memory resources.

In contrast to the claimed embodiments, Applicants understand Zucker to teach *a single* processor accessing *a single* memory module (col. 12, lines 23-32; col. 10, lines 41-48). However, this does not amount to a teaching of *a plurality of processors* accessing *a plurality of memory resources* as claimed. Additionally, Zucker fails to teach or suggest a plurality of processors *simultaneously* accessing a plurality memory resources as claimed. Further, Zucker fails to teach or suggest each of the processors simultaneously accessing

a different memory resource as claimed. Accordingly, Applicants reiterate that Zucker fails to teach or suggest the limitations of "wherein said first resource controller is further operable to enable each of said plurality of processors to simultaneously access a different memory resource of said plurality of memory resources" as recited in Claim 30, and similarly recited in Claim 39.

Applicants respectfully submit that Zucker fails to teach or suggest the limitations of "wherein said second resource controller is further operable to enable each of said plurality of processors to simultaneously access a different peripheral resource of said plurality of peripheral resources" as recited in Claim 31, and similarly recited in Claim 40. As recited and described in the present application, the second resource controller is operable to enable each of the plurality of processors to simultaneously access a different peripheral resource of the plurality of peripheral resources.

In contrast to the claimed embodiments, Applicants understand Zucker to teach that a processor can be locked to a plurality of device ports at the same time (col. 11, lines 34-35). However, *a single processor* locked to a plurality of device ports is very different from *a plurality of processors* accessing a plurality of peripheral resources as claimed. Additionally, Zucker fails to teach or suggest a plurality of processors *simultaneously* accessing a plurality peripheral resources as claimed. Further, Zucker fails to teach or suggest each of the processors simultaneously accessing *a different peripheral resource* as claimed. Accordingly, Applicants reiterate that Zucker fails to teach or suggest the

limitations of "wherein said second resource controller is further operable to enable each of said plurality of processors to simultaneously access a different peripheral resource of said plurality of peripheral resources" as recited in Claim 31, and similarly recited in Claim 40.

For these reasons, Applicant respectfully submits that independent Claim 28 is neither anticipated nor rendered obvious by Zucker, thereby overcoming the 35 U.S.C. §102(b) rejection of record. Since independent Claim 37 recites limitations similar to those discussed above with respect to independent Claim 28, independent Claim 37 also overcomes the 35 U.S.C. §102(b) rejection of record. Since dependent Claims 29-33, 35, 38-42 and 44 recite further limitations to the invention claimed in their respective independent Claims, Claims 29-33, 35, 38-42 and 44 are also neither anticipated nor rendered obvious by Zucker. Therefore, Claims 28-33, 35, 37-42 and 44 are allowable.

Claims 46-50

Claims 46-50 are rejected in the present Office Action under 35 U.S.C. §102(b) as being anticipated by Zucker. Applicants have reviewed the cited reference and respectfully submit that the embodiments of the present invention as recited in Claims 46-50 are neither anticipated nor rendered obvious by Zucker for the following reasons.

Applicant respectfully directs the Examiner to independent Claim 46, which recites a controller for negotiating access to a plurality of shared resources comprising (emphasis added):

> a plurality of shared resource controllers, wherein each of said plurality of shared resource controllers is operable to simultaneously communicate with a different shared resource of a plurality of shared resources;
>
> a plurality of dedicated buses, wherein each of said plurality of dedicated buses is coupled to a respective shared resource controller of said plurality of shared resource controllers, and wherein each of said plurality of dedicated buses is further operable to couple to a respective shared resource of said plurality of shared resources; and
>
> a resource arbitration controller for controlling access of a plurality of processors to said plurality of shared resources, wherein said resource arbitration controller is further operable to control at least one switching component for coupling a processor of said plurality of processors to at least one shared resource controller of said plurality of shared resource controllers, and wherein said resource arbitration controller is further operable to control said at least one switching component based upon a priority value assigned to said processor.

Claims 47-50 depend from independent Claim 46 and recite further limitations to the claimed invention.

Applicants respectfully submit that Zucker fails to teach or suggest the limitations of "a plurality of shared resource controllers," "a plurality of dedicated buses" and "a resource arbitration controller for controlling access of a plurality of processors to said plurality of shared resources" as recited in independent Claim 46. As recited and described in the present application, a controller includes a plurality of shared resource controllers, a plurality of dedicated buses and a resource arbitration controller for controlling access of a plurality of processors to the plurality of shared resources.

Assuming arguendo that memory controller (MC) 80 or device controller (DC) 82 as taught by Zucker is analogous to a controller as claimed, Applicants respectfully submit that Zucker fails to teach that MC 80 or DC 82 include a plurality of shared resource controllers as claimed. Additionally, Applicants respectfully submit that Zucker fails to teach that MC 80 or DC 82 include a plurality of dedicated buses as claimed. Further, Applicants respectfully submit that Zucker fails to teach that MC 80 or DC 82 include a resource arbitration controller for controlling access of a plurality of processors to the plurality of shared resources as claimed. Accordingly, Applicants reiterate that Zucker fails to teach or suggest the limitations of "a plurality of shared resource controllers," "a plurality of dedicated buses" and "a resource arbitration controller for controlling access of a plurality of processors to said plurality of shared resources" as recited in independent Claim 46.

For these reasons, Applicant respectfully submits that independent Claim 46 is neither anticipated nor rendered obvious by Zucker, thereby overcoming the 35 U.S.C. §102(b) rejection of record. Since dependent Claims 47-50 recite further limitations to the invention claimed in their respective independent Claims, Claims 47-50 are also neither anticipated nor rendered obvious by Zucker. Therefore, Claims 46-50 are allowable.

Claim Rejections – 35 U.S.C. §103

Claims 34 and 43

Claims 34 and 43 are rejected in the present Office Action under 35 U.S.C. §103(a) as being unpatentable over Zucker in view of United States Patent Number 5,949,982 to Frankeny et al. (referred to herein as "Frankeny"). Applicant has reviewed the cited references and respectfully submits that the embodiments of the present invention as recited in Claims 34 and 43 are not rendered obvious by Zucker in view of Frankeny for the following reasons.

Applicants respectfully submit that Frankeny, either alone or in combination with Zucker, fails to cure the deficiencies of Zucker discussed herein. More specifically, Applicants respectfully submit that Frankeny also fails to teach or suggest the limitations of "wherein said first resource controller is further operable to implement respective buses for coupling said plurality of processors to said plurality of memory resources" and "wherein said first resource controller is further operable to implement respective buses for coupling said plurality of processors to said plurality of peripheral resources" as recited in independent Claim 28, and similarly recited in independent Claim 37. Accordingly, independent Claims 28 and 37 are not rendered obvious by Zucker in view of Frankeny. Since dependent Claims 34 and 43 recite further limitations to the invention claimed in their respective independent Claims, Claims 34 and 43 are also not rendered obvious by Zucker in view of Frankeny. Therefore, Claims 34 and 43 are allowable.

Claims 36, 45 and 51

Claims 36, 45 and 51 are rejected in the present Office Action under 35 U.S.C. §103(a) as being unpatentable over Zucker. Applicant has reviewed the cited reference and respectfully submits that the embodiments of the present invention as recited in Claims 36, 45 and 51 are not rendered obvious by Zucker for the following reasons.

Page 4 of the rejection takes official notice of the limitations "wherein said plurality of memory resources, said plurality of peripheral resources, said plurality of processors, said memory controller, and said peripheral controller comprise components of a portable electronic device" as recited in Claim 36, and similarly recited in Claims 45 and 51. Applicants respectfully disagree with this assertion and direct the Examiner to MPEP §2144.03(E), which states that "[i]t is never appropriate to rely solely on common knowledge in the art without evidentiary support in the record as the principal evidence upon which a rejection was based." Additionally, as stated in MPEP §2144.03(C): "'[T]he Board [or examiner] must point to some concrete evidence in the record in support of these findings' to satisfy the substantial evidence test. If the examiner is relying on personal knowledge to support the finding of what is known in the art, the examiner must provide an affidavit or declaration setting forth specific factual statements and explanation to support the finding." Accordingly, Applicants respectfully invite the Examiner to provide documentary evidence in the next Office Action if the rejection is to be maintained (see MPEP §2144.03(C); see 37 CFR §1.104(c)(2)).

Furthermore, Applicants respectfully submit that independent Claims 28, 37 and 46 are neither anticipated nor rendered obvious by Zucker for the reasons discussed herein. Since dependent Claims 36, 45 and 51 recite further limitations to the invention claimed in their respective independent Claims, Claims 36, 45 and 51 are also not rendered obvious by Zucker in view of Frankeny. Therefore, Claims 36, 45 and 51 are allowable.

CONCLUSION

Applicants respectfully submit that Claims 28-51 are in condition for allowance and Applicants earnestly solicit such action from the Examiner.

The Examiner is urged to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 50-4160.

Respectfully submitted,

MURABITO, HAO & BARNES LLP

Dated: 9 / 24 / 2008 /BMF/

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